Symwave SW3080 v.CD Silicon Errata

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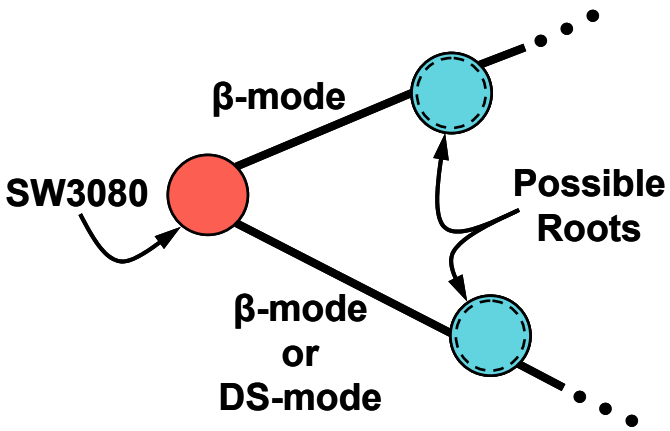
SILICON ERRATA ID	PROBLEM DESCRIPTION	RESOLUTION / WORK-AROUNDS
1. Gap-before-Ack Issue	Symptom If the SW3080 is not root and repeats between two other nodes and at least one of the connections is a β-mode connection, then asynchronous data transfers have a small chance of a Gap event being indicated before an Acknowledge (Ack) packet is transmitted. The result is the Ack packet being ignored and the data packet being retransmitted; slightly lower Asynchronous data throughput will result. Occurrences This issue only occurs in β-only or Hybrid networks with three or more nodes. It does not occur in two-node networks and DS-mode (only) networks. It only occurs if the SW3080 is not root.  	A. Setting the gap count to 10 (decimal) or higher greatly reduces the probability of this issue occurring. Many systems leave the gap count at 0x3F, which is excessively long and some systems set the gap count to 0x01, which is generally too short. B. Set the SW3080 to be the root of the network.

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2. PHY-Link Disable Issue	Symptom To disable the PHY-Link interface the LPS signal is deasserted (held logic zero) for a period of $T_{LPS-DISABLE}$. In the SW3080 PHY, the LPS signal has an additional low pulse-width requirement ($T_{LPS-DISL}$) of 1 mSec. Occurrences If there are one or more active ports on the SW3080 then the issue will not occur. If all of the SW3080 ports are unconnected, disabled, in standby or suspended then the issue occurs when the Link Layer Controller (LLC) wants to disable the PHY-Link interface, such as going into a low-power mode. When the LLC wants to disable the PHY-Link interface, the LLC holds the LPS signal logic zero for a $T_{LPS-DISABLE}$ period. The SW3080 PHY clock output turns off correctly within the $T_{LPS-DISABLE}$ period. However, an addition $T_{LPS-DISL}$ LPS low period is required. The total $T_{LPS-DISL}$ period is 1 mSec. Since the SW3080 PHY-Link interface will be disabled then according to the IEEE-1394b specification the LLC must wait a $T_{LPS-ENABLE}$ period of up to 10 mSec before communications resume with the SW3080. The actual SW3080 $T_{LPS-ENABLE}$ period is 2.3 mSec. Therefore the worst-case LPS disable / re-enable is 1 mSec + 2.3 mSec = 3.3 mSec. It should be noted that PHY-Link interface resets done by asserting the LPS signal logic zero for a period of $T_{LPS-RESET}$ works as specified in the IEEE-1394b specification. The $T_{LPS-RESET}$ period is 2.75 µSec (maximum).	No work-around exists. The effect on system performance is minimal because disabling and re-enabling the PHY-Link interface requires the LLC wait up to 10 mSec regardless of the actual $T_{LPS-DISABLE}$ / T_{LPS_DISL} / $T_{LPS-ENABLE}$ periods.

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